Amendment to the Specification

WP 10.16.09 **The Paragraph beginning at Page ~~311~~ 307 to Page 308 Line 2, lines 18~~23~~, is to be amended as follows:**

20.14.13.1.1 Non-CPU Read Data Coherency

Note that for data coherency reasons, a non-CPU read will always result in read data being returned to the requester which includes the after-effects of any pending (i.e. pre-arbitrated, but not yet executed) non-CPU write to the same address, which is currently cached in the non-CPU write buffer. ~~This is shown graphically in Figure n page319 on page Error! Bookmark not defined.~~

WP 10.16.09 **The Paragraph beginning at Page ~~416~~ 411, lines ~~35~~ 8-39 through to Page 417, lines 1-2, is to be amended as follows:**

Consequently, the higher the resolution of the TFS the more printed dots can be printed for each *macrodot*, where a macrodot represents a single data bit of the tag. The more dots that are available to produce a macrodot, the more complex the pattern of the macrodot can be. ~~As an example, Figure n page161 on page Error! Bookmark not defined. shows the~~The Netpage tag structure is rendered such that the data bits are represented by an average of 8 dots × 8 dots (at 1600 dpi), but the actual shape structure of a dot is not square. This allows the printed Netpage tag to be subsequently read at any orientation.

WP 10.16.09 **The Paragraph beginning at Page ~~441~~ 435, lines ~~1~~ 17-20, is to be amended as follows:**

~~As can be seen from Figure n page488 on page Error! Bookmark not defined. there~~ There are 3 stages of muxing between the Tag Data register and the RS encoders or 2D decoders. Levels 1-2 are controlled by *level1_mux* and *level2_mux* which are generated within the TDi FSM as is the write address to the ETDi buffers (*etd_wr_adr*)

WP 10.16.09 **The Paragraph beginning at Page ~~445~~ 440, lines ~~8~~ 6-9, is to be amended as follows:**

~~The implementation of the circuit can be seen in Figure~~ The main components are XOR gates, 4-bit shift registers and multiplexers.

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The Paragraph beginning at Page ~~480~~ 474, lines ~~13-21~~ 5-13, is to be amended as follows:

The ink replacement mechanism has 6 ink replacement patterns, one per ink plane, programmable by the CPU. The dead nozzle mask is ANDed with the dot data to see if there are any planes where the dot is active but the corresponding nozzle is dead. The resultant value forms an enable, on a per ink basis, for the ink replacement process. If replacement is enabled for a particular ink, the values from the corresponding replacement pattern register are ORed into the dot data. The output of the ink replacement process is then filtered so that error diffusion is only allowed for the planes in which error diffusion is enabled. The output of the ink replacement logic is ORed with the resultant dot after dead nozzle removal. ~~See Figure 4 page565 on page Error! Bookmark not defined. for implementation details.~~